AMENDMENTS TO THE CLAIMS

Claims 1-9 (Cancelled.)

10. (Original) A method of forming a MOS transistor on a semiconductor material of a first conductivity type, the method comprising the steps of:

forming a layer of material of the first conductivity type on the semiconductor material, the layer of material having silicon, germanium, and carbon;

forming an insulation layer over the layer of material;

forming a layer of conductive material on the insulation layer;

etching the layer of conductive material to form a gate; and

forming spaced-apart source and drain regions of a second conductivity type in the layer of material on opposite sides of the gate.

11. (Original) The method of claim 10 wherein the forming a layer of material step includes the step of growing the layer of material on the semiconductor material.

12. (Original) The method of claim 10 wherein the forming a layer of material step includes blanket depositing a layer of silicon germanium carbon over the semiconductor material.

13. (Original) The method of claim 10 wherein

an isolation region adjoins the semiconductor material, the isolation region having a top surface; and

the forming a layer of material step includes the step of selectively epitaxially growing the layer of material on the semiconductor material, the layer of material having a top surface that lies below the top surface of the isolation region.

14. (Original) The method of claim 13 wherein the semiconductor material has a bottom surface that is substantially coplanar with the top surface of the isolation region.

15. (Original) The method of claim 10 wherein the forming a layer of material step includes the steps of:

removing a portion of the semiconductor material to expose an etched surface of the semiconductor material; and

growing the layer of material on the etched surface of the semiconductor material.

16. (Original) The method of claim 10 wherein the forming a layer of material step includes the steps of:

removing a portion of the semiconductor material to expose an etched surface of the semiconductor material; and

blanket depositing a layer of silicon germanium carbon over the etched surface of the semiconductor material.

17. (Original) The method of claim 12 wherein the forming a layer of material step includes the steps of:

removing a portion of the semiconductor material to expose an etched surface of the semiconductor material, the etched surface of the semiconductor material lying below the top surface of the isolation region; and

epitaxially growing the layer of material on the etched surface of the semiconductor material.

18. (Original) The method of claim 15 and further comprising the step of forming a layer of cap silicon on the layer of material prior to the formation of the insulation layer.

19. (Original) The method of claim 10 wherein the layer of material has a substantially uniform concentration of carbon atoms.

20. (Original) The method of claim 10 wherein the layer of material has a non-uniform concentration of carbon atoms, and includes a surface region of a heavy concentration of carbon.

21. (New) A method of forming a MOS transistor, the method comprising the steps of:

forming a region of a first conductivity type;

forming an insulation layer over the region;

forming a layer of conductive material on the insulation layer;

etching the layer of conductive material to form a gate; and

forming spaced-apart source and drain regions of a second conductivity type in the region on opposite sides of the gate.

22. (New) The method of claim 21 and further comprising a semiconductor material of the first conductivity type, the region contacting the semiconductor material and lying between the semiconductor material and the insulation layer.

23. (New) The method of claim 22 wherein the semiconductor material is a well in a substrate of the second conductivity type.

24. (New) The method of claim 23 wherein the region includes silicon, germanium, and carbon.

25. (New) The method of claim 22 wherein the region includes silicon, germanium, and carbon.

26. (New) The method of claim 21 wherein the region includes a top surface, and a layer of carbon formed at the top surface.

27. (New) The method of claim 26 wherein the region includes silicon and germanium.

28. (New) The method of claim 22 wherein the forming a region step includes the steps of:

removing a portion of the semiconductor material to expose an etched surface of the semiconductor material; and

growing a layer of material on the etched surface of the semiconductor material to form the region.

29. (New) The method of claim 22 wherein the forming a region step includes the steps of:

removing a portion of the semiconductor material to expose an etched surface of the semiconductor material;

blanket depositing a layer of silicon germanium carbon over the etched surface of the semiconductor material to form the region; and

planarizing the layer of silicon germanium carbon to form the region.